Proof-of-concept for post-OFDM waveforms as candidates for 5G

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***Abstract*—Beyond the current state-of-the-art orthogonal frequency division multiplexing (OFDM), new waveforms are foreseen as key enablers for a highly flexible air interface that addresses the heterogeneous requirements of advanced 5G services. In this context, three promising candidate waveforms are demonstrated using real-time hardware platform: Flexible Configured (FC)-OFDM, Universal-Filtered (UF)-OFDM, and Filter Bank Multi-Carrier (FBMC). The presented work was undertaken in the context of the H2020 European Fantastic-5G research project, in collaboration between IMT Atlantique, Orange Labs, and Nokia Bell Labs.**

The demonstration illustrates how we were able to reduce the hardware complexity of these new waveforms (by careful analysis of the signal properties and original scheduling of the computations), which becomes mostly equivalent to state-of-the-art OFDM used in 4G. This is done while bringing new opportunities to enable 5G scenarios such as vehicular communications with high velocity of user device and Machine type communications with relaxed synchronization. Key performance metrics are measured and evaluated with respect to state-of-the-art OFDM, such as robustness against Doppler and synchronization errors, hardware complexity, and throughput.

EXTENDED ABSTRACT

On board validation is a crucial step to fully validate any proposed algorithm or hardware architecture. This is particularly the case when multiple techniques are competing to meet specific application needs, as it is the case in waveform design for the new radio air interface in the upcoming 5th generation (5G) of mobile communication systems. The 5G standard is foreseen to support multiple new services while coexisting with the typical mobile broadband service of 4G/Long Term Evolution (LTE). For internet-of-things applications, massive Machine-Type Communication (MMC) service is introduced, adding specific requirements such as the support of relaxed synchronization. Other applications, like Mission Critical Communications (MCC), require the support of low-latency communication. Lastly, Vehicular communication applications (V2X) imposes the support of reliable communication with very high mobility.

To support these services, multiple waveform parameters on the same carrier (often referred to as numerology) may be required, which raises the issue of their coexistence. Therefore, novel waveforms have been designed and proposed for the upcoming 5G standard to answer these new challenges. Filter-Bank Multi-Carrier with Offset-Quadrature Amplitude Modulation (FBMC/OQAM) and Universal Filtered-OFDM (UF-OFDM) are two of the most promising waveforms. Theoretical analysis in the literature demonstrated the superiority of these new waveform with respect to OFDM for the upcoming 5G scenarios [1][2]. Therefore, it is of high interest to prove these results and to validate the benefits of the proposed waveforms through real hardware implementations and radio frequency transmissions.

In this context, the current demonstration presents one of the first flexible and efficient hardware platforms for waveform design proof-of-concept (PoC). Part of this platform has been developed in the context of the H2020 European Fantastic-5G research project [3]. The proposed platform constitutes a complete hardware/software development environment: digital processing boards based on Field Programmable Gate Array (FPGA) and an embedded dual-core ARM cortex A9 processor, radio frequency boards, and all associated interfaces for control, communication, and display. FBMC/OQAM, FC-OFDM, and UF-OFDM transceivers, in addition to OFDM, are implemented with careful architectural choices to allow fair comparisons. Furthermore, the demonstration illustrates how the proposed flexible platform can support MMC, V2X, and MCC scenarios. Performance results in terms of Bit-Error-Rate (BER) are presented and discussed, together with corresponding hardware complexity results.

The proposed platform environment is presented in Fig. 1 where one board (Xilinx ZedBoard) emulates a user equipment (UE) at transmitter side, and a second board (Xilinx ZC706 evaluation board) is used to emulate the base-station (BS) at receiver side. These two digital processing boards are based on the recent Zynq-7000 System-on-Chip (SoC) which integrates a dual-core ARM Cortex A9 processor and a reconfigurable logic fabric (FPGA). Both boards are extended by a radio-frequency (RF) front-end (Analog Devices AD-FMCOMMS1-EBZ) to enable radio transmissions. Each of these RF boards integrates one transmit and one receive interface. The transmit interface of the BS is optionally used to emulate a multi-user environment for demonstration purpose. On-board control and communication interfaces are ensured by the embedded dual-core Cortex A9 processor. The considered modulation techniques are implemented in hardware on the FPGA part of the Zynq-7000 SoC.

In addition to these boards, two host computers are used for control and results display purpose. They run two dedicated LabVIEW Graphical User Interfaces (GUI). The GUI at the transmitter side is used to select the target scenario, the waveform parameters, and the image to transmit. It displays in addition the power spectral density corresponding to the selected waveform parameters. At the receiver side, the GUI displays relevant performance metrics, such as BER, received constellation and received image data. Furthermore, both GUIs display metrics related to the hardware complexity and throughput.

As illustrated in Fig. 1 ⓐ multiple parameters can be selected using the GUI at the transmitter side (TX): target scenario, QAM constellation, type of waveform, type of filter for FBMC/OQAM, etc. The user can also select between several images to transmit.

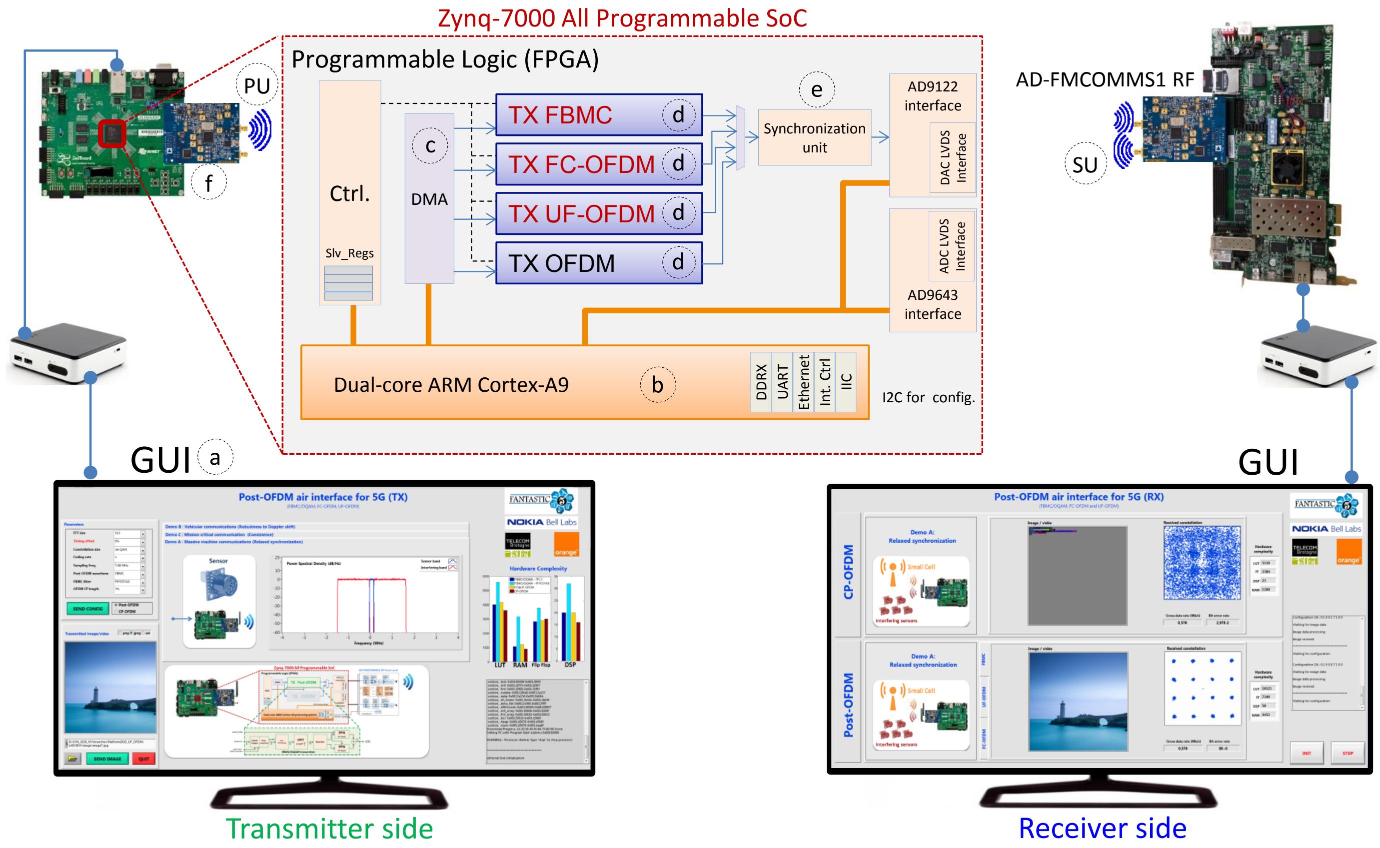

Fig. 1. Demonstration setup with front-end interface.

TABLE I
WAVEFORM PARAMETERS

Parameter	Value	
	Config. 1	Config. 2
FFT size	512	256
Sampling rate	7.68 MHz	
Constellation	16-QAM	
CP length	36	18
Filter length (UF-OFDM)	37	19
Filter type (UF-OFDM)	Dolph-chebyshev, sidelobe level of 70 dB	
Prototype filter (FBMC)	TFL1 [4] or PHYDYAS [5]	
Equalizer	Zero forcing	
Channel estimation	Least square	

For transmitting the control data, the ARM ⓑ executes sequentially the first three tasks defined above. For transmitting the image data, tasks 1), 4) then 5) are executed. When the data are transferred via the DMA ⓒ, they are processed by the unit in the FPGA ⓓ related to the selected waveform. Then, the output waveform samples are sent to a synchronization unit ⓔ. This latter inserts an impulse signal before these samples. At the same time, it transmits a synchronization signal (denoted by *sync*) through a wire directly connected to the receiver board. This signal enables, at the receiver side, to correct the timing offset introduced by the channel.

Lastly, the output waveform samples are sent to the RF board for digital to analog conversion, amplification, and modulation ⓕ.

Example of the considered waveform parameters are summarized in Table I. Two configurations are demonstrated:

- config. 1 corresponds to a typical 4G/LTE numerology,
- config. 2 corresponds to a set of parameters where the symbol duration is halved when compared to config. 1.

Measured BER demonstrates how the candidate waveforms clearly outperform OFDM in the considered scenarios, confirming state-of-the-art theoretical results. Hardware synthesis results [6][7] show that the required hardware resources for most of the candidate waveforms are close to that of OFDM at the transmitter side. Therefore, with the recently proposed optimizations and hardware PoC, the hardware complexity becomes no longer a discriminating factor for most of those 5G candidate waveforms.

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