Demo: Tracking loop of a GPS receiver under noisy hardware

Mohamed Mourad Hafidhi*, Imran Wali*, Sushant S. Samuel†, Arnaud Dion‡ and Emmanuel Boutillon*
*Lab-STICC, UMR 6582, Université de Bretagne Sud, 56100 Lorient, France.
†Indian Institute of Technology Roorkee, India
‡ISAE, Toulouse, France

***Abstract*—Global Positioning System (GPS) receivers are heavily used in mobile contexts, and there is motivation to minimize power consumption and maximize battery life in these devices. Power consumption and device lifetime can be improved by operating at minimal supply voltage, which increases the likelihood of hardware errors. The loss of robustness increases with the advancement of CMOS technology in combination with process/voltage/temperature (PVT) variations. The RELIASIC (Reliable ASIC) project investigates the fault tolerance in the GPS context starting from a standard GPS application and adding some redundant mechanisms to allow the GPS receiver to be tolerant to hardware errors. An Application-specific integrated circuit (ASIC) will be designed with two versions of the GPS receiver: the standard version, and a complex version where fault tolerant techniques are added to make the GPS receiver more tolerant to hardware errors. This demo presents the FPGA platform used to implement the two versions of the GPS receivers. The computed positions of the GPS affected by several type of noise are displayed on a screen with google map.**

I. Introduction

Global Positioning System (GPS) receivers are heavily used in mobile contexts, and there is motivation to minimize power consumption and maximize battery life in these devices. Power consumption and device lifetime can be improved by operating at minimal supply voltage, which increases the likelihood of hardware errors. The loss of robustness increases with the advancement of CMOS technology in combination with process/voltage/temperature (PVT) variations [1].

The RELIASIC (Reliable ASIC) project [2] investigates the fault tolerance in the GPS context starting from a standard GPS application (extracted and modified from [**?**]) and adding some redundant mechanisms to allow the GPS receiver to be tolerant to hardware errors due to low voltage supply. An Application-specific integrated circuit (ASIC) is designed with two versions of the GPS receiver: the standard version, and a complex version where fault tolerant techniques are added to make the GPS receiver more tolerant to hardware errors (including, previous authors work [3], [4], [5], [6]). This demo presents the platform used first to implement the standard GPS receiver algorithm, and, then to evaluate the performance and the hardware complexity of a proposed technique for error tolerance. This platform (see Fig. 1, 2) will be used to test the future ASIC.

Fig. 1. Photograph of the FPGA test setup

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