SiPS 2017

IEEE International Workshop on Signal Processing Systems
Lorient, France, Oct. 3-5 2017
www.sips2017.org

Extended Paper submission deadline: **May 11th 2017**
Acceptance notification: **June 27th 2017**
Camera ready: **July 13th 2017**

IEEE SiPS is a premier international forum collecting researchers and practitioners from industry and academia for exchanging the latest scientific and technical advances in the area of design and implementation of signal processing systems. It addresses current and future challenges and new directions in research and development of these systems. Prospective authors are invited to submit manuscripts on topics including, but not limited to:

Software Based Design and Implementation of Signal Processing Systems
- Software solutions on programmable digital signal processors and systems
- Application specific instruction-set processor (ASIP) architectures and systems
- SIMD, VLIW and multi-core CPU architectures
- Graphics processing unit (GPU) based massively parallel implementations
- Embedded FPGA architectures

Hardware Based Design and Implementation of Signal Processing Systems
- Low-power signal processing circuits and applications
- High performance VLSI systems
- VLSI designs for 100 Gbps and beyond networking systems
- FPGA and reconfigurable architecture based systems
- System-on-chip and network-on-chip
- VLSI systems for wireless sensor network and RF identification systems

Emerging Technologies
- Vehicular ad hoc networks (VANET)
- Cognitive radio networks
- Internet of Things (IoT)
- Deep learning and reconfigurable/ASIC processors
- Bio-inspired networks
- Context-aware mobile networking
- Wireless body area networks (WBANs)
- Implantable communications
- Tele-medicine/e-health networks

Signal Processing Application Systems
- Audio, speech and language processing
- Biomedical signal processing and bioinformatics
- Image, video and multimedia signal processing
- Information forensics, security and cryptography
- Machine learning for signal processing
- Sensing and sensor signal processing
- Autonomous energy harvesting-based sensor networks
- Signal processing for non-volatile memory system
- Latency and power constrained signal processing techniques for high-speed networking
- Wireless communications and networking
- Coding and compression
- Multiple-input-multiple-output (MIMO) and communication systems
- Software defined radio

Signal Processing Compensation Techniques for Mixed-Signal Technologies
- Digital compensation techniques for variations in silicon process, temperature, aging
- Error detection and correction for volatile and non-volatile memories
- Power reduction and SNR improvement for on-chip, off-chip interconnects and buses
- Digital compensation signal processing for ADCs, power-amps, MEMS, power controllers

Design Methods of Signal Processing Algorithms and Architectures
- Optimization of signal processing algorithms
- Compilers and tools for signal processing systems
- Algorithm transformation and algorithm-to-architecture mapping
- Dataflow based design methodologies
- Error-tolerant techniques for signal processing

Paper Submission: Authors are invited to submit full-length (max. 6 pages), original, unpublished papers. Previously published papers or papers currently under review for other conferences/journals should not be submitted and will not be considered. Paper format information is available at **www.sips2017.org**.

IEEE SiPS 2017 has a special theme: "**Reliable signal processing systems**". Future Signal Processing applications and systems will have to consider reliability in addition to pursuing optimal performance. Submissions that fall into this inter-disciplinary area are particularly encouraged.

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